WHAT IS CLAIMED IS:

- 1 1. A transistor, comprising:
- 2 a workpiece;
- a doped region disposed in the workpiece, the doped region including a dopant species;
- a doped gate dielectric disposed over the doped region of the workpiece, the doped gate
- 5 dielectric including the dopant species;
- a gate disposed over the gate dielectric; and
- a source region and a drain region formed in at least the doped region of the workpiece,
- 8 wherein the source region, drain region, gate, and doped gate dielectric comprise a transistor.
- 1 2. The transistor according to Claim 1, wherein the dopant species comprises at least one
- 2 Group V, VI or VII element.
- 1 3. The transistor according to Claim 2, wherein the dopant species comprises nitrogen or
- 2 fluorine.
- 1 4. The transistor according to Claim 1, wherein the doped region comprises a thickness of
- 2 about 100 Å or less.
- 1 5. The transistor according to Claim 1, wherein the dopant species fills vacancies in the
- 2 atomic structure of the gate dielectric.
- 1 6. The transistor according to Claim 1, wherein the doped gate dielectric comprises a high k
- 2 dielectric material or an oxide, and wherein the gate comprises a semiconductor material or a
- 3 metal.

- 1 7. The transistor according to Claim 6, wherein the doped gate dielectric comprises about 50
- 2 Å or less of Si₃N₄, Al₂O₃, Ta₂O₅, HfO₂, TiO₂, HfSiO_x, ZrO₂, or ZrSiO_x.
- 1 8. The transistor according to Claim 1, further comprising a thin insulating layer disposed
- 2 between the gate dielectric and the doped region of the workpiece.
- 1 9. The transistor according to Claim 8, wherein the thin insulating layer comprises a
- 2 thickness of about 10 Å or less.
- 1 10. The transistor according to Claim 9, wherein the thin insulating layer comprises silicon
- 2 dioxide or silicon oxynitride.
- 1 11. The transistor according to Claim 1, wherein the workpiece comprises a silicon-on-
- 2 insulator (SOI) wafer.

- 1 12. A method of fabricating a transistor, the method comprising:
- 2 providing a workpiece;
- 3 introducing a dopant species into the workpiece to form a doped region in the workpiece;
- depositing a gate dielectric material over the doped region of the workpiece;
- 5 depositing a gate material over the gate dielectric material;
- 6 patterning the gate material and gate dielectric material to form a gate and a gate
- 7 dielectric over the doped region of the workpiece;
- 8 transferring the dopant species from the workpiece to the gate dielectric material to form
- 9 a doped gate dielectric material; and
- forming a source region and a drain region in at least the doped region of the workpiece,
- wherein the source region, drain region, gate, and doped gate dielectric comprise a transistor.
- 1 13. The method according to Claim 12, wherein introducing the dopant species comprises
- 2 introducing at least one dopant species comprising a Group V, VI or VII element into the
- 3 workpiece.
- 1 14. The method according to Claim 13, wherein introducing the dopant species into the
- 2 workpiece to form the doped region includes introducing nitrogen or fluorine into the workpiece.
- 1 15. The method according to Claim 12, wherein introducing the dopant species into the
- 2 workpiece to form the doped region comprises implanting ions of the dopant species into the
- 3 workpiece.
- 1 16. The method according to Claim 15, wherein implanting the ions of the dopant species
- 2 comprises an energy level of about 5 KeV or less.

- 1 17. The method according to Claim 15, wherein implanting the ions of the dopant species
- 2 comprises an implantation dose of about 1×10^{14} to 1×10^{15} ions/cm².
- 1 18. The method according to Claim 12, wherein transferring the dopant species from the
- 2 workpiece to the gate dielectric material comprises an anneal process.
- 1 19. The method according to Claim 18, wherein the anneal process comprises a temperature
- 2 of about 900 to 1050 °C.
- 1 20. The method according to Claim 18, wherein the anneal process comprises a spike anneal
- 2 process or a rapid thermal anneal (RTA) process.
- 1 21. The method according to Claim 18, wherein the anneal process comprises an anneal
- 2 process to form the source region and the drain region, or a separate anneal process.
- 1 22. The method according to Claim 21, wherein the separate anneal process is performed
- 2 after depositing the gate dielectric material, after depositing the gate material, or after patterning
- 3 the gate material and the gate dielectric material.
- 1 23. The method according to Claim 12, wherein introducing the dopant species into the
- 2 workpiece to form the doped region comprises forming a doped region having a thickness of
- 3 about 100 Å or less.
- 1 24. The method according to Claim 12, wherein depositing the gate dielectric material
- 2 comprises forming vacancies in the atomic structure of the gate dielectric material, and wherein
- 3 transferring the dopant species from the workpiece to the gate dielectric material comprises
- 4 filling the vacancies of the gate dielectric material.

- 1 25. The method according to Claim 12, wherein depositing the gate dielectric material
- 2 comprises depositing a high k dielectric material or an oxide, and wherein depositing the gate
- 3 material comprises depositing a semiconductor material or a metal.
- 1 26. The method according to Claim 12, wherein depositing the gate dielectric comprises
- 2 depositing about 50 Å or less of Si₃N₄, Al₂O₃, Ta₂O₅, HfO₂, TiO₂, HfSiO_x, ZrO₂, or ZrSiO_x.
- 1 27. The method according to Claim 12, wherein depositing the gate dielectric comprises
- 2 atomic layer deposition (ALD), chemical vapor deposition (CVD), or metal oxide CVD
- 3 (MOCVD).
- 1 28. The method according to Claim 12, further comprising forming a thin insulating layer
- 2 over the doped region of the workpiece, before introducing the dopant species into the workpiece
- 3 to form the doped region.
- 1 29. The method according to Claim 28, wherein forming the thin insulating layer comprises
- 2 depositing an insulating layer having a thickness of about 100 Å or less.
- 1 30. The method according to Claim 28, wherein forming the thin insulating layer comprises
- 2 forming silicon dioxide or silicon oxynitride.
- 1 31. The method according to Claim 28, further comprising removing at least a portion of the
- 2 thin insulating layer, after introducing the dopant species into the workpiece to form the doped
- 3 region.

- 1 32. The method according to Claim 31, wherein about 10 Å or less of the thin insulating
- 2 layer remains over the doped region of the workpiece, after removing at least the portion of the
- 3 thin insulating layer.
- 1 33. The method according to Claim 31, wherein removing at least a portion of the thin
- 2 insulating layer comprises removing all of the thin insulating layer.
- 1 34. The method according to Claim 12, wherein providing the workpiece comprises
- 2 providing a silicon-on-insulator (SOI) wafer.
- 1 35. The method according to Claim 12, further comprising, before depositing the gate
- 2 dielectric material:
- depositing a dummy gate material over the workpiece;
- patterning the dummy gate material with the pattern of the gate;
- 5 forming the source region and the drain region; and
- 6 removing the dummy gate material.
- 1 36. The method according to Claim 35, wherein introducing the dopant species into the
- 2 workpiece to form a doped region is performed either before or after forming the source region
- 3 and the drain region.